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INTERDIGITATED CAPACITOR AND METHOD FOR FABRICATION THEROF

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The Invention relates generally to capacitors formed within integrated circuits. More particularly, the invention relates to capacitors with enhanced capacitance formed within integrated circuits.

2. Description of the Related Art

[0002] Capacitors find common use in integrated circuits as signal transduction components as well as data storage components. A common goal when fabricating capacitors within integrated circuits is to form capacitors with enhanced capacitance within limited semiconductor substrate surface area. Under such circumstances, integrated circuit die may often be fabricated with enhanced performance and reduced size.

[0003] Current approaches to forming higher capacitance capacitors provide multi-layer capacitor structures within minimized substrate area. While effective in providing increased capacitance, additional improvements in capacitance are nonetheless desirable. The present invention is directed towards that object.

SUMMARY OF THE INVENTION

[0004] A first object of the invention is to provide a capacitor for use within a microelectronic product.

[0005] A second object of the invention is to provide a capacitor in accord with the first object of the invention, where the capacitor is formed with enhanced capacitance.

[0006] In accord with the objects of the invention, the invention provides a capacitor for use within a microelectronic product, and a method for fabricating the capacitor.

[0007] A capacitor fabricated in accord with the invention is fabricated over a substrate. A first capacitor plate layer is formed from a first conductor layer having a first series of horizontally separated and interconnected tines that define a series of apertures interposed therebetween. A capacitor dielectric layer is formed upon the first conductor layer without completely filling the series of apertures. A second conductor layer is formed upon the capacitor dielectric layer and completely filling the series of apertures interposed between the first series of tines. The second conductor layer may be partially or completely planarized to form a second capacitor plate layer with a second series of tines horizontally interdigitated with the first series of tines.

[0008] The invention provides a capacitor with enhanced capacitance for use within a microelectronic product.

[0009] The invention realizes the foregoing object by forming the capacitor with a first capacitor plate layer having a first series of interconnected tines such that a second series of

tines within a second capacitor plate layer may be horizontally interdigitated with the first series of tines.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The objects, features and advantages of the invention are understood within the context of the Description of the Preferred Embodiment, as set forth below. The Description of the Preferred Embodiment is understood within the context of the accompanying drawings, which form a material part of this disclosure, wherein:

[0011] Fig. 1, Fig. 2, Fig. 3, Fig. 4 and Fig. 5 show a series of schematic cross-sectional diagrams illustrating the results of progressive stages in fabricating a capacitor structure in accord with a first preferred embodiment of the invention.

[0012] Fig. 6 shows a schematic plan-view diagram corresponding with Fig. 5.

[0013] Fig. 7, Fig. 8, Fig. 9, Fig. 10 and Fig. 11 show a series of schematic cross-sectional diagrams illustrating the results of progressive stages in fabricating a capacitor structure in accord with a second preferred embodiment of the invention.

[0014] Fig. 12 shows a schematic perspective-view diagram corresponding with Fig. 11.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0015] The invention provides a capacitor with enhanced capacitance for use within a microelectronic product.

[0016] The invention realizes the foregoing object by forming the capacitor with a first capacitor plate layer having a first series of interconnected tines such that a second series of tines within a second capacitor plate layer may be horizontally interdigitated with the first series of tines.

[0017] Fig. 1 to Fig. 5 show a series of schematic cross-sectional diagrams illustrating the results of progressive stages in fabricating a microelectronic product in accord with a first preferred embodiment of the invention.

[0018] Fig. 1 first shows a substrate 10 having a contact region 12 formed therein.

[0019] The substrate 10 may comprise any of several types of substrates conventionally employed within microelectronic products. Such substrates may include but are not limited to semiconductor substrates and ceramic substrates. Representative semiconductor substrates include bulk silicon semiconductor substrates, bulk silicon-germanium alloy semiconductor substrates and semiconductor-on-insulator semiconductor substrates. Typically, the substrate 10 includes a semiconductor substrate having a dielectric surface layer laminated thereover.

[0020] The contact region 12 may be either a conductor contact region or a semiconductor contact region depending upon the layered nature of the substrate 10.

[0021] A pair of patterned first dielectric layers 14a and 14b is formed upon the substrate 10 and defining a first aperture that accesses the contact region 12. The pair of patterned first dielectric layers 14a and 14b may be formed from any of several dielectric materials, including generally higher dielectric constant dielectric materials (having a dielectric constant of from about 4 to about 8, such as silicon oxide, silicon nitride and silicon oxynitride dielectric materials) and generally lower dielectric constant dielectric materials (having a dielectric constant of less than about 4, such as spin-on-glass (SOG), spin-on-polymer (SOP), amorphous carbon and fluorosilicate glass (FSG) dielectric materials). Typically, each of the pair of patterned first dielectric layers 14a and 14b is formed to a thickness of from about 4000 to about 8000 angstroms.

[0022] Finally, Fig. 1 shows a series of series of patterned first conductor layers 18a, 18b, 18c and 18d nested within a series of patterned first barrier layers 16a, 16b, 16c and 16d, in turn separated by a series of patterned second dielectric layers 20a, 20b and 20c.

[0023] The series of patterned dielectric layers 20a, 20b and 20c may in general be formed of dielectric materials analogous, to the dielectric materials that are employed for forming the

pair of patterned first dielectric layers 14a and 14b. For reasons that will become clearer below, they are not formed of identical dielectric materials. Each of the series of patterned second dielectric layers 20a, 20b and 20c is typically formed to a thickness of from about 4000 to about 8000 angstroms. The series patterned first conductor layers 18a, 18b, 18c and 18d is typically formed of a copper or copper alloy conductor material. The series of patterned first barrier layers 16a, 16b, 16c and 16d is typically formed from any of several barrier materials appropriate for inhibiting interdiffusion of the series of patterned first conductor layers 18a, 18b, 18c and 18d with the series of patterned first dielectric layers 20a, 20b and 20c. Such barrier materials may include, but are not limited to titanium barrier materials, tungsten barrier materials and nitride alloys thereof. Typically, each of the series of patterned barrier layers 16a, 16b, 16c and 16d is formed to a thickness of from about 200 to about 500 angstroms. As is illustrated in Fig. 1, the patterned barrier layer 16b and the patterned first conductor layer 18b connect to the contact region 12.

[0024] Fig. 1 implicitly illustrates a microelectronic product having a series of patterned conductor layers formed employing a planarizing method and separated by a series of patterned dielectric layers. The invention is not so limited. Directly patterned conductor layers may also be employed within the invention. Aluminum containing conductor materials are often directly patterned while employing plasma etch methods.

Copper containing conductor materials are typically not readily plasma etchable, thus requiring planarizing methods.

[0025] Fig. 1 finally shows the substrate 10 as divided into a peripheral region Rp and a capacitor region Rc. A capacitor in accord with the invention will be formed within the capacitor region Rc.

[0026] Fig. 2 shows the results of forming a patterned photoresist layer 22 upon the patterned barrier layer 16a, the patterned conductor layer 18a and patterned dielectric layer 20a, thus covering the peripheral region Rp of the substrate 10 but not the capacitor region Rc of the substrate 10. The patterned photoresist layer 22 may be formed of positive photoresist materials or negative photoresist materials. Typically, the patterned photoresist layer 22 is formed to a thickness of from about 10000 to about 20000 angstroms.

[0027] Fig. 3 first shows the results of stripping the pair of patterned dielectric layers 20b and 20c from interposed between the series of patterned conductor layers 18b, 18c and 18d to form a pair of second apertures 23a and 23b. Fig. 3 next shows the results of stripping the patterned photoresist layer 22 from upon the patterned barrier layer 16a, the patterned conductor layer 18a and the patterned dielectric layer 20a.

[0028] The foregoing sequential stripping may be effected employing etchants as are conventional in the microelectronic product fabrication art. A hydrofluoric acid based etchant may

be employed to strip the pair of patterned second dielectric layers 20b and 20c when formed of a silicon oxide based dielectric material. The patterned photoresist layer 22 may be stripped employing wet chemical and/or dry plasma strippers.

[0029] Fig. 4 shows the results of successively layering: (1) a blanket capacitor dielectric layer 24; (2) a blanket second barrier layer 26; and (3) a blanket second conductor layer 28 upon the microelectronic product of Fig. 3. The blanket capacitor dielectric layer 24 incompletely fills the pair of second apertures 23a and 23b, while the blanket second conductor layer 28 completely fills the pair of second apertures 23a and 23b.

[0030] The blanket capacitor dielectric layer 24 may be formed of capacitor dielectric materials as are conventional in the microelectronic product fabrication art. They may include generally lower dielectric constant capacitor dielectric materials (i.e., having a dielectric constant less that about 8, such as silicon oxide, silicon nitride and silicon oxynitride dielectric materials) and generally higher dielectric constant capacitor dielectric materials (i.e., having a dielectric constant of greater than about 8, such as lead zirconate titanate and barium strontium titanate dielectric materials). The blanket capacitor dielectric layer 24 is typically formed to a thickness of from about 20 to about 200 angstroms. The blanket second barrier layer 26 may be formed of materials and dimensions analogous, equivalent or identical to the materials and dimensions employed for forming the series of patterned

first barrier layers 16a, 16b, 16c and 16d. The blanket second conductor layer 28 may be formed of materials and dimensions analogous, equivalent or identical to the materials and dimensions employed for forming the series of patterned first conductor layers 18a, 18b, 18c and 18d.

[0031] Fig. 5 shows the results of planarizing the microelectronic product of Fig. 4 while employing the blanket capacitor dielectric layer 24 as a planarizing stop layer. The planarizing provides a pair of patterned second conductor layers 28a and 28b nested within a pair of patterned second barrier layers 26a and 26b formed within the pair of second apertures 23a and 23b.

[0032] Fig. 6 shows a schematic plan-view diagram of the microelectronic product of Fig. 5.

[0033] Fig. 6 shows a patterned second conductor layer 28a/b nested within a patterned second barrier layer 26a/b in turn planarized within the blanket capacitor dielectric layer 24. Shown in phantom outline beneath the blanket capacitor dielectric layer 24 is the patterned first conductor layer 18a nested within the patterned first barrier layer 16a. Also shown in phantom is the patterned first conductor layer 18b/c/d nested within the patterned first barrier layer 16b/c/d. As is illustrated within Fig. 5 and Fig. 6, the patterned first conductor layer 18b/c/d is formed in the shape of a comb with the series of tines 18b, 18c and 18d horizontally separated by the pair of second apertures 23a and 23b. The patterned second

conductor layer 28a/b fills the pair of second apertures 23a and 23b and provides a pair of second tines horizontally (and not vertically) interdigitated with the series of first tines.

[0034] As illustrated in Fig. 5 and Fig. 6, a capacitor in accord with the invention is formed employing a self aligned planarizing method for forming a patterned first capacitor plate layer 28a/b with respect to a patterned second capacitor plate layer 18b/c/d. Under circumstances where the pair of second apertures 23a and 23b as illustrated in Fig. 3 is formed with a minimum photolithographically resolvable linewidth, a patterned second conductor layer 28a or 28b is formed with less than a minimum photolithographically resolvable linewidth. In addition, the invention also provides direct thickness control when depositing a capacitor dielectric layer. In light of the foregoing features, the invention provides a capacitor with enhanced capacitance within a reduced substrate area.

[0035] The invention also provides a characteristic serpentine shaped contiguous capacitor dielectric layer 24. It is formed in sequence: (1) covering a top surface of a patterned first conductor layer; (2) interposed between a pair of opposing sidewalls of the patterned first conductor layer and a patterned second conductor layer; (3) beneath a bottom surface of the patterned second conductor layer; and (4) interposed between a pair of opposing sidewalls of the patterned second conductor layer and an additional patterned first conductor layer.

[0036] Fig. 7 to Fig. 11 show a series of schematic cross-sectional diagrams illustrating the results of progressive stages in forming a microelectronic product in accord with a second preferred embodiment of the invention.

[0037] Fig. 7 is identical with Fig. 1. Identical layers and identical structures are numbered identically.

[0038] Fig. 8 corresponds with Fig. 2, but with the addition of a blanket extrinsic planarizing stop layer 21 formed upon the microelectronic product of Fig. 7 and beneath the patterned photoresist layer 22. Otherwise, identical layers and identical structures are numbered identically.

[0039] Fig. 9 corresponds with Fig. 3, but with the addition of a patterned extrinsic planarizing stop layer 21a covering the patterned first barrier layer 16a, the patterned first conductor layer 18a and the patterned second dielectric layer 20a. Otherwise, identical layers and identical structures are numbered identically.

[0040] Fig. 10 corresponds with Fig. 4, but also with the addition of a patterned extrinsic planarizing stop layer 21a covering the patterned first barrier layer 16a, the patterned first conductor layer 18a and the patterned second dielectric layer 20a. Otherwise, identical layers and identical structures are numbered identically.

[0041] Fig. 11 corresponds with Fig. 5, but illustrates an incomplete planarization of the blanket second conductor layer 28 over the capacitor region Rc to form an incompletely planarized second conductor layer 28' upon an incompletely planarized second barrier layer 26' upon an incompletely planarized capacitor dielectric layer 24'. In addition to completely filling the pair of second apertures 23a and 23b, the incompletely planarized second conductor layer 28' also covers top portions of the series of patterned first conductor layers 18b, 18c and 18d, thus providing for enhanced capacitance.

[0042] Fig. 12 shows a partially exploded schematic perspective-view diagram of Fig. 11. Absent is the peripheral region of the substrate 10, the partially planarized barrier layer 26' and the partially planarized capacitor dielectric layer 24'. Fig. 12 clearly shows the partially planarized second conductor layer 28' that serves as a second capacitor plate horizontally and not vertically interdigitated with and covering a series of top surfaces of the series of patterned first conductor layers 18b, 18c and 18d.

[0043] The preferred embodiment of the invention is illustrative of the invention rather than limiting of the invention. Revisions and modifications may be made to methods, materials structures and dimensions in accord with the preferred embodiments of the invention, while still providing a microelectronic product in accord with the invention, further in accord with the accompanying claims.